PHASE NOISE PERFORMANCE COMPARISON BETWEEN LIGA-MEMS AND ON-CHIP CMOS CAPACITORS FOR A VCO APPLICATION

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Abstract

An integrated voltage-controlled oscillator using TSMC 0.18 μm CMOS technology is presented to demonstrate and compare the phase noise performance between the VCO using a new type of MEMS variable capacitor and that using conventional CMOS varactor, which is built on-chip together with the CMOS VCO. A representative MEMS variable capacitor, fabricated using the LIGA process, has a nominal capacitance of 1.05 pF and exhibits a Q factor of 40.9 at 2.7 GHz. The simulation results show that with this LIGA-MEMS capacitor, a 4.3 dB of phase noise improvement at 300 kHz offset from the carrier is achieved when the VCO operates at 2.7 GHz.

Keywords— *CMOS, LIGA, micro-eletromechanical system (MEMS), variable capacitors, voltage-controlled oscillator (VCO)*

1 Introduction

Modern communication systems have an increasing demand on high performance RF and microwave circuits and devices. Among them, the voltage-controlled oscillator (VCO) is one of the important components. VCOs have been widely used in many different RF circuits and have been studied for a long time [1, 2]. Although a lot of work has been done, VCO design is still challenging, because of the increasing need for high performance applications at higher frequencies. The difficulty in designing low phase noise VCOs is that high quality factor (Q factor) passive components, such as inductors and varactors are difficult to achieve in standard silicon processes for high frequencies applications [3]. The phase noise of an oscillator is inversely proportional to the square of the Q factor of the resonator [4]. Thus, improving the Q factor of the components in the resonator is a critical issue.

In recent years, micro-electromechanical systems (MEMS) devices have been receiving increasing attention as the replacement for on-chip passive elements, and various MEMS tunable capacitor designs have been reported [5, 6]. Some of the designs use parallel plates, where the capacitance is varied by changing the gap between the plates, while the others use a lateral comb structure, in which the overlap of the capacitor fingers is adjusted to change the capacitance.

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This paper presents a VCO using a new type of MEMS variable capacitor, which is built using deep X-ray lithography (LIGA) process. The parallel plates of the capacitor are oriented perpendicular to the substrate. This type of capacitors exhibit high quality factor at microwave frequencies. The designed VCO, using the TSMC 0.18 μm CMOS process, can connect either to an on-chip CMOS varactor or the off-chip LIGA-MEMS capacitor as the frequency tuning component. Phase noise simulation results are presented to demonstrate the advantage of the high-Q LIGA-MEMS capacitor over the conventional CMOS varactor.

2 LIGA-MEMS Capacitor

LIGA-MEMS variable capacitors have been designed and simulated using ANSYS™ [7] and Ansoft HFSS™ [8], and representative simulation results have been previously reported [9]. A typical LIGA-MEMS variable capacitor, shown in Fig. 1, consists of a thin grounded vertical cantilever positioned between two electrodes. When a DC bias voltage is applied between the actuator electrode and the cantilever, the cantilever is pulled towards the actuator electrode. This action decreases the capacitance between the capacitance electrode and the cantilever. This three plate capacitor design permits an increase in tuning range over a two plate capacitor [10].

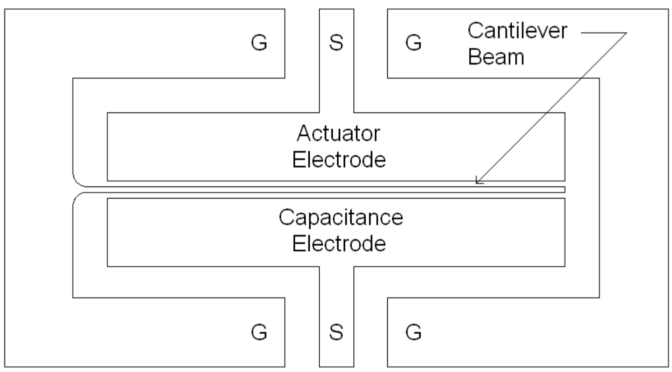

Figure 1: LIGA-MEMS Variable Capacitor

One of the LIGA-MEMS variable capacitor designs has been fabricated using the LIGA process at Forschungszentrum Karlsruhe (FZK), a national laboratory in Germany. Samples were processed by IMT (Institute for Microstructure Technology), including the X-ray exposure at the FZK storage ring ANKA. The substrate used was a 1 mm thick alumina wafer with a 3 μm oxidized titanium seed layer and a 150 μm layer of PMMA (polymethyl methacrylate) photoresist. This sample was exposed to X-rays through a mask consisting of 20 μm thick gold absorbers on a 2.7 μm thick titanium membrane. Following the irradiation, the exposed resist was developed with GG developer. The voids in the resist were filled with electro-plated nickel to a thickness of 100 μm. The remaining resist was then flood exposed and removed using another step of development. The structure was then descummed in oxygen plasma and wet etched with 5% HF acid for 2 minutes to remove the seed layer, electrically isolating the capacitor structures. This isotropic etching also underetches all structures, selectively releasing the thin beam, while still providing good adhesion of the large metal parts.

The fabricated devices have layouts and functionalities that are very similar to the devices given in [9]. The fabricated devices (100 μm nickel) are shorter than the presented simulation results (350 μm nickel) for an initial fabrication attempt. Preliminary test results of the fabricated capacitor show a Q factor of 40.9 and a capacitance of 1.05 pF at 2.7 GHz, which is the operational frequency of the VCO. Simulation results of the same structure show a Q factor of 120.9 and a capacitance 1.14 pF at 2.7 GHz. The difference between measured and simulated results is believed to be due to suboptimal excitation of the tall LIGA structures with standard planar wafer probes.

3 VCO Design and Integration

To exemplify some potential advantages of the LIGA-MEMS capacitors, a cross-coupled VCO using TSMC 0.18 μm CMOS technology was designed using Cadence® Virtuoso® [11], for fabrication on a 1 mm^2 CMOS chip. The 3.3 V VCO is designed to operate from 2.6 GHz to 2.7 GHz. The tuning component can be either a CMOS varactor, which is built on the same chip as the VCO core, or an off-chip LIGA-MEMS variable capacitor described in the previous section.

Fig. 2 shows a circuit schematic of the VCO core. Transistors M0 and M1 act as negative resistors to compensate the loss in the passive LC tank. M3 and M4 are used as a buffer stage to isolate the LC tank from the 50 Ω output terminal. The two on-chip spiral inductors (L0 and L1) were designed and simulated using the ASITIC software [12]. The on-chip varactor consists a combination of a fixed MIM (metal-insulator-metal) capacitor and NMOS varactors. Since the MIM capacitor has less parasitic resistance than NMOS varactor, this design can achieve higher Q factor than the one built completely with NMOS varactors with the trade-off in tuning range.

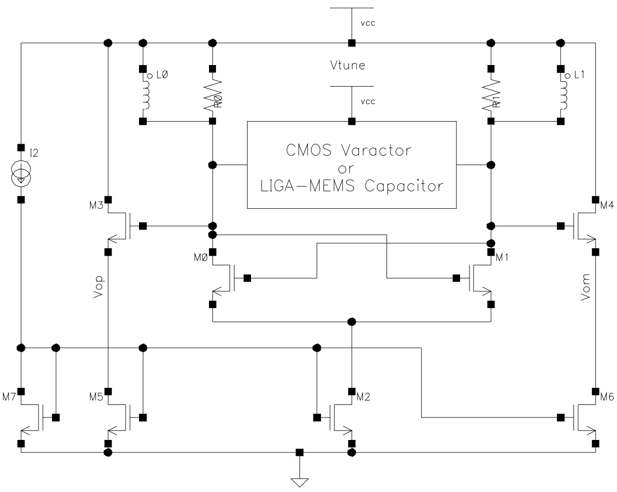

Figure 2: Cadence Schematic for VCO Core

A challenge in this project is in integrating the LIGA-MEMS capacitor with the CMOS chip. Since the LIGA-MEMS capacitor was not specifically designed for this particular VCO application, no external connection is available on the LIGA-MEMS capacitor. A proposed method for integration is wire bonding the pins of the CMOS chip to certain solid areas on the LIGA-MEMS capacitor. The bonding wires introduce parasitic inductance and resistance to the system, thus affecting the operation frequency and reducing the overall Q factor of the LC-tank. Models of bonding wires were included in simulation for both MEMS capacitor and on-chip capacitor to ensure a fair comparison. However, the advantage of LIGA-MEMS capacitor in phase noise is more obvious if the effect of bonding wires is minimized.

Other integration approaches are possible. One is to introduce connection pads to the LIGA-MEMS capacitor, designed to match the CMOS pads. Flip-chip packaging technology could be used to make it possible to solder the pads directly, thus avoiding bonding wires. Another method is to build the LIGA-MEMS capacitor and the CMOS VCO on the same substrate but two different areas, and connected by build-in connection wires. The CMOS and LIGA process would be done separately, thus one area must be properly protected while the other area is under process.

4 Results and Discussion

Phase noise analysis was simulated using Agilent® ADS® [13]. Two VCO models were used. The first one uses a CMOS varactor model extracted from Cadence®, the second one uses a LIGA-MEMS capacitor model derived from tested data for the representative fabricated LIGA-MEMS capacitor. As shown in Fig. 3, at the 2.7 GHz operation frequency, the two VCO models have phase noise of -103.5 dBc/Hz and -107.8 dBc/Hz respectively at a 300 kHz offset. An improvement of 4.3 dB is observed.

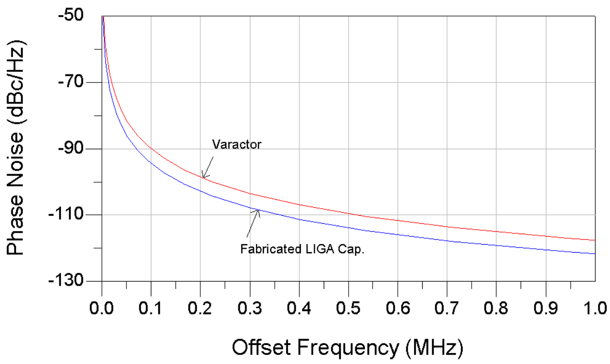

Figure 3: Phase Noise for 2 VCOs

It is theoretically possible to further improve the VCO phase noise performance. Simulation indicates that the Q factor of similar LIGA-MEMS capacitors can reach up to 520 at 2.7 GHz if copper is used instead of nickel, compared to the fabricated test capacitor with Q factor of 40.9 in this study. Many other factors, such as the Q factor of the inductors in the resonator, bonding wires, and the transistor tail current also contribute to the phase noise [14]. Optimizing these factors may further reduce the phase noise.

Table I summarizes the phase noise comparison of this work and a few other CMOS VCOs recently reported. The VCO using the representative LIGA-MEMS capacitor has comparably good phase noise performance.

The LIGA-MEMS capacitor has further potential in VCO applications. Its high self-resonant frequency and high Q factor at upper-microwave frequency allows it to keep good performance in circuits running at even higher frequency, when CMOS passive elements may lose their desired electrical properties. Simulation shows that the VCO using the representative LIGA-MEMS capacitor model has a phase noise below -100 dBc/Hz at 300 kHz offset at 4.2 GHz.

TABLE I
Phase Noise of Several Comparable CMOS VCOs

Reference	Freq. (GHz)	PN @300kHz (dBc/Hz)
On-Chip Varactor (This work)	2.7	-103.5
Fab. LIGA-MEMS Cap. (This work)	2.7	-107.8
On-Chip MEMS Ind. [15]	2.6	-117
Quadrature VCO [16]	2.45	-105
PMOS Varactor [17]	2.5	-110

5 Conclusions

With the newly developed MEMS variable capacitor using the LIGA process, a high Q factor passive component has been combined with high frequency CMOS circuits to improve phase noise performance. A VCO has been designed using TSMC 0.18 μm CMOS technology to evaluate the improvement over the conventional CMOS varactor. Simulation results at 2.7 GHz show that the VCO using the CMOS on-chip varactor has a phase noise of -103.5 dBc/Hz at 300 kHz offset from the carrier frequency. The VCO using the representative fabricated LIGA-MEMS variable capacitor has a phase noise of -107.8 dBc/Hz at 300 kHz offset. The phase noise performance is improved with the LIGA-MEMS capacitor, but limited primarily by the low Q factor on-chip inductor, the bonding wires between the CMOS chip and MEMS capacitor, and the transistor tail current. Further improvement is possible with improved designs.

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